What Is Claimed Is:

1. A fail repair circuit of a nonvolatile ferroelectric memory device having a repair logic unit therein, the fail repair circuit comprising:

a memory test logic block generating a redundancy active pulse (RAP) if a row address including a fail bit to be repaired is found during test;

a power-up sensor generating a power-up pulse if a stable power source voltage is sensed;

a first redundancy control block generating first to fifth control signals ENN, ENP, EQN, CPL, and PREC and a sixth control signal ENW in response to the RAP and the power-up pulse;

a counter generating n bit counter bit signal increased by one bit through the RAP to correspond to the number of redundancy bits;

a redundancy counter decoding control block generating an activated coding signal ENW<n> in response to the counter bit signal of the counter and the sixth control signal ENW; and

a redundancy coding block outputting a master signal in response to the coding signal ENW<n> and the first to fifth control signals, programming a fail address in a plurality of redundancy coding cells, and outputting seventh and eighth control signals REN<n> and RPUL<n> to repair the programmed fail address.

2. The circuit according to claim 1, further comprising a counter output coding bus that codes the counter bit signal output from the counter to output the counter bit signal to the redundancy counter decoding control block; and a first operational block consisting of a plurality of operation units that perform logic AND operation of the coding signal from the counter output coding bus and invert the resultant value.

3. The circuit according to claim 1, wherein the redundancy counter decoding control block includes:

first to nth redundancy counter decoding control blocks, each redundancy counter decoding control block including:

a first inverter block consisting of a plurality of inverters inverting an output signal of each NAND gate of the first NAND gate block;

a second operation block consisting of a plurality of operation units performing logic AND operation of an output signal of each inverter of the first inverter block and the sixth control signal ENW of the first redundancy control block and inverting the resultant value; and

a second inverter block consisting of a plurality of inverters inverting an output signal of each operation unit of the second operation block and outputting the activated coding signal ENW<n>.

4. The circuit according to claim 1, wherein the redundancy coding block includes:

a redundancy master cell outputting a master signal that determines whether to activate or inactivate the whole redundancy coding cells in response to the first to fifth control signals ENN, ENP, EQN, CPL, and PREC from the first redundancy control block and the activated coding signal ENW<n>;

a redundancy coding cell block having a plurality of redundancy coding cells arranged in a row direction to store an actual fail address, in response to the first to fourth control signals and the activated coding signal ENW<n>;

a third operation block performing logic OR operation of an output signal according to on/off state of the redundancy coding cells and inverting the resultant value;

a first inverter inverting a signal of the third operation block and outputting a seventh signal REN<n>;

a second inverter inverting a signal of the first inverter and outputting an eighth signal RPUL<n>; and

PMOS transistors respectively arranged in final output terminals of the redundancy coding cells connected in a row direction.

5. The circuit according to claim 4, wherein the redundancy coding cell includes:

a first signal transport means transferring a power source voltage VCC to a first node N1 in response to the second control signal ENP;

a first latch having one node connected with the first node N1 and the other node connected with second and third nodes N2 and N3;

a first NMOS switch S1 controlling whether to connect the second node N2 with the third node N3 in response to the third control signal EQN;

a second signal transport means having a gate terminal to which the sixth control signal ENW is input, a source terminal to which a signal of the second node N2 is transferred, and a drain terminal to which the first address signal ADD is input;

a third signal transport means having a gate terminal to which the coding signal ENW<n> is input, a source terminal to which the second address signal is input, and a drain terminal to which a signal of the third node N3 is transferred;

fourth and fifth signal transport means turned on/off depending on the first and second address signals ADD and ADDB;

a sixth signal transport means transferring the ground voltage VSS to a fourth node N4 in response to the first control signal ENN;

a second latch having one node connected with the fourth node N4 and the other node connected with fifth and sixth nodes N5 and N6;

a first ferrorelectric capacitor FC1 arranged between an input node of the fourth control signal CPL and the fifth node N5;

a second ferroelectric capacitor FC2 arranged between the input terminal of the fourth control signal CPL and the sixth node N6;

a third ferroelectric capacitor FC3 arranged between the fifth node N5 and the ground voltage terminal VSS;

a fourth ferroelectric capacitor FC4 arranged between the sixth node N6 and the ground voltage terminal VSS; and

seventh and eighth signal transport means turned on/off under the control of signals of the fifth and sixth nodes N5 and N6.

6. The circuit according to claim 4, wherein the redundancy master cell includes:

a ninth signal transport means transferring the power source voltage VCC to a seventh node N7 in response to the second control signal ENP;

a third latch having one node connected with the seventh node N7 and the other node connected with eighth and ninth nodes N8 and N9;

a second NMOS switch S2 controlling whether to connect the eighth node N8 with the ninth node N9 in response to the third control signal EQN;

a tenth signal transport means having a gate terminal to which the coding signal ENW<n> is input, a drain terminal to which a signal of the eighth node N8 is transferred, and a source terminal to which the power source voltage is input;

an eleventh signal transport means having a gate terminal to which the sixth control signal ENW is input, a source terminal to which a signal of the ninth node N9 is transferred, and a drain terminal to which the ground voltage VSS is input;

a twelfth signal transport means transferring the ground voltage VSS to a tenth node N10 in response to the first control signal ENN;

a fourth latch having one node connected with the tenth node N10 and the other node connected with eleventh and twelfth nodes N11 and N12;

a fifth ferroelectric capacitor FC5 arranged between the input terminal of the fourth control signal CPL and the eleventh node N11;

a sixth ferroelectric capacitor FC6 arranged between the input node of the fourth control signal CPL and the twelfth node N12;

seventh and eighth ferroelectric capacitors FC7 and FC8 arranged in parallel between the eleventh node N11 and the ground voltage terminal VSS;

a ninth ferroelectric capacitor FC9 arranged between the twelfth node N12 and the ground voltage terminal VSS; and

thirteenth and fourteenth signal transport means arranged in series between an output terminal of the master signal and the ground voltage terminal under the control of the eleventh node N11 and the fifth control signal PREC.

7. The circuit according to claim 1, further comprising:

a second redundancy control block outputting a ninth signal DECDIS to inactivate a normal predecoder path in response to the eighth control signal RPUL<n> and at the same time outputting a tenth control signal REDEN to control driving of a redundancy wordline/plate line driver intended to be used as a redundancy cell;

a predecoder block outputting an eleventh control signal DEC<n> activated by activating only a path that can be used as a redundancy circuit, in response to the seventh and ninth control signals;

a post decoder block outputting a post decoder signal Post DEC<n> activated in response to the activated eleventh control signal DEC<n>;

the redundancy wordline/plate line driver activating a corresponding wordline/plate line in response to the tenth and eleventh control signals REDEN and DEC<n>; and

a redundancy cell array block activating a corresponding redundancy cell in response to the activated signal of the redundancy wordline/plate line driver.

8. The circuit according to claim 7, wherein the second redundancy control block includes:

a fourth operation block consisting of a plurality of third input operation units performing logic OR operation of the eighth control signal and inverting the resultant value;

a fifth operation block performing logic AND operation of the operation units of the fourth operation block;

a third inverter IN3 inverting an output signal of the fifth operation block and outputting a ninth control signal DECDIS to activate only a predecoder path that can be used as a redundancy circuit; and

a fourth inverter IN4 inverting the signal of the third inverter IN3 and outputting a tenth control signal REDEN.

9. The circuit according to claim 7, wherein the predecoder block includes a plurality of predecoders, each of the predecoders including:

a sixth operation block consisting of a plurality of operation units performing logic AND operation of a first row address, a second row address, and the ninth control signal DECDIS and inverting the resultant value;

a seventh operation block consisting of a plurality of operation units performing logic AND operation of an output signal of each operation unit of the

sixth operation block and the seventh control signal REN<n> and inverting the resultant value; and

a plurality of delay blocks D0~Dn delaying and outputting an output signal of each operation unit of the seventh operation block.

10. A method for repairing fail of a nonvolatile ferroelectric memory device having a repair logic unit therein, the method comprising the steps of:

generating a redundancy active pulse (RAP) if a row address including a fail bit to be repaired is found during test;

generating a power-up pulse if a stable power source voltage is sensed;

generating first to fifth control signals ENN, ENP, EQN, CPL, and PREC and a sixth control signal ENW in response to the RAP and the power-up pulse, the first to fifth control signals controlling a redundancy coding block and the sixth control signal controlling a redundancy counter decoding control block;

generating n bit counter bit signal increased by one bit through the RAP to correspond to the number of redundancy bits;

generating an activated coding signal ENW<n> corresponding to the fail bit in response to the counter bit signal of the counter and the sixth control signal ENW;

programming a fail bit(address) in the redundancy coding block including a redundancy master cell and a redundancy coding cell, each having ferroelectric capacitors, in response to the first to fifth control signals ENN, ENP, EQN, CPL, and PREC and the activated coding signal ENW<n>; and

outputting seventh and eighth control signals REN<n> and RPUL<n> to repair the programmed fail address.

11. The method according to claim 10, wherein the fail repairing is performed during an active period where a chip enable signal is activated at low level and a period where the fifth control signal PREC is maintained at high level.

12. The method according to claim 10, wherein the first control signal ENN is maintained at high level while the second third control signals EPN and EQN are maintained at low level when the fail is repaired.

13. The method according to claim 10, wherein the fail address is coded in such a manner that the coding signal ENW<n> is maintained at high level, the fourth control signal PREC is output at high level, the redundancy master cell outputs a master signal of low level, and first and second output terminals RS1 and RS2 of

the respective redundancy coding cells in a row direction are connected with each other.

14. The method according to claim 13, further comprising the steps of:

outputting a ninth control signal DECDIS to a predecoder block to activate only a predecoder output path that can be used as a redundancy circuit, in response to the eighth control signal RPUL<n> output from the redundancy coding block if the programmed fail bit(address) is input;

outputting a tenth control signal REDEN which is an inverted signal of the ninth control signal DECDIS;

outputting an eleventh control signal DEC<n> to the predecoder block to activate a row address corresponding to the fail bit(address) among a plurality of row addresses of the redundancy cell array block in response to the seventh control signal REN<n> and the ninth control signal DECDIS;

outputting a twelfth control signal Post DEC<n> which is an activated post decoder signal, to a redundanch wordline/plate line driver to correspond to the fail bit(address) in response to the eleventh control signal DEC<n>; and

outputting the row address active signal corresponding to the fail bit(address) to the redundancy cell array block in response to the tenth and twelfth control signals REDEN and Post DEC<n>.

15. The method according to claim 10, wherein the first and second output terminals of the redundancy coding cell are connected with each other in case of the fail column address of high level in such a manner that the coding signal ENW<n> and the fourth control signal CPL are maintained at high level if the programmed fail address is input, the first address signal ADD and one node of a first ferroelectric capacitor are maintained at high level, and the second address signal ADDB and one node of a second ferroelectric capacitor are maintained at low level.

16. The method according to claim 10, wherein the first and second output terminals of the redundancy coding cell are connected with each other in case of the fail address of low level in such a manner that the coding signal ENW<n> and the fourth control signal CPL are maintained at high level if the programmed fail address is input, the first address signal ADD and one node of a first ferroelectric capacitor are maintained at low level, and the second address signal ADDB and one node of a second ferroelectric capacitor are maintained at low level.